25W AccuSwitch™ AC/DC Controller with Integrated 700V Power FET Optimized for > 5V Applications with Option for Input OVP

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1 Description

The iW1825 is an ***AccuSwitch™*** product that integrates a 700V power MOSFET with a high-performance digital AC/DC controller. The product offers a unique light load mode that can be configured with an external resistor to allow the design to be optimized for ultra-low no-load power consumption or fast transient response. It operates in quasi-resonant mode to provide high efficiency at heavy loads and minimizes the external component count while simplifying EMI design and lowering the total bill of material cost.

Dialog's ***PrimAccurate™*** primary-side sensing technology allows the iW1825 to eliminate the need for secondary-side feedback while achieving excellent line and load regulation. This proprietary digital control technology also eliminates the need for loop compensation components while maintaining stability over all operations. Pulse-by-pulse waveform analysis allows for a loop response that is much faster than traditional solutions, resulting in improved dynamic load response. The built-in power limit function enables optimized transformer design in universal off-line applications and allows for a wide input voltage range.

Dialog's innovative proprietary technology ensures that power supplies built with the iW1825 can achieve both the highest average active efficiency and less than 75mW no-load power consumption. Active start-up circuitry enables fast, yet smooth start-up into large capacitive loads at output voltages of 9V, 12V or higher, making it ideal for networking and monitor adaptor applications.

The iW1825 offers a full range of fault protection circuits including internal and external over-voltage protection (OVP). The external OVP feature can monitor either the input voltage or output voltage. The -01 and -31 options offer a supplemental output OVP, while the -10 option can monitor the input voltage, even during start-up, to protect from an over-voltage event on the input.

2 Features

- ***AccuSwitch*** technology - integrated 700V power MOSFET
- 25W output power capable
- iW1825-01 and iW1825-31 options: external supplemental output over-voltage protection, optimized for 9V+ output voltages
- iW1825-10 options: external input over-voltage protection, supports 5V+ output voltages
- Adaptively controlled soft-start enables fast and smooth start-up into large capacitive loads (from 330µF to 6,000µF) at 9V+ output voltages
- Internal single-point fault protections against output short-circuit, output over-voltage and output over-current
- User-configurable light-load operation mode for optimized dynamic load response and no-load power consumption
- < 75mW no-load power consumption at $230V_{AC}$ with fast dynamic load response in typical 12V, 2A 24W compact adapter/charger
- ***PrimAccurate™*** Primary-side feedback eliminates optocouplers and simplifies design
- Proprietary optimized 79kHz maximum PWM switching frequency with quasi-resonant operation achieves best size, efficiency and common mode noise
- ***EZ-EMI®*** design enhances manufacturability
- Adaptive multi-mode PWM/PFM control improves efficiency
- User-configurable 5-level cable drop compensation provides design flexibility in iW1825-01 and iW1825-31 options
- Tight constant-voltage and constant current regulation across line and load range
- ***SmartDefender™*** smart hiccup technology helps to address issues of soft shorts in cables and connectors by effectively reducing the average output power at fault conditions without latch
- Optional on-chip internal over-temperature protection
- No audible noise over entire operating range
- 10-lead SOIC batwing package

3 Applications

- Power adapters for network devices and monitors
- Universal AC/DC adapters (5 – 25W)

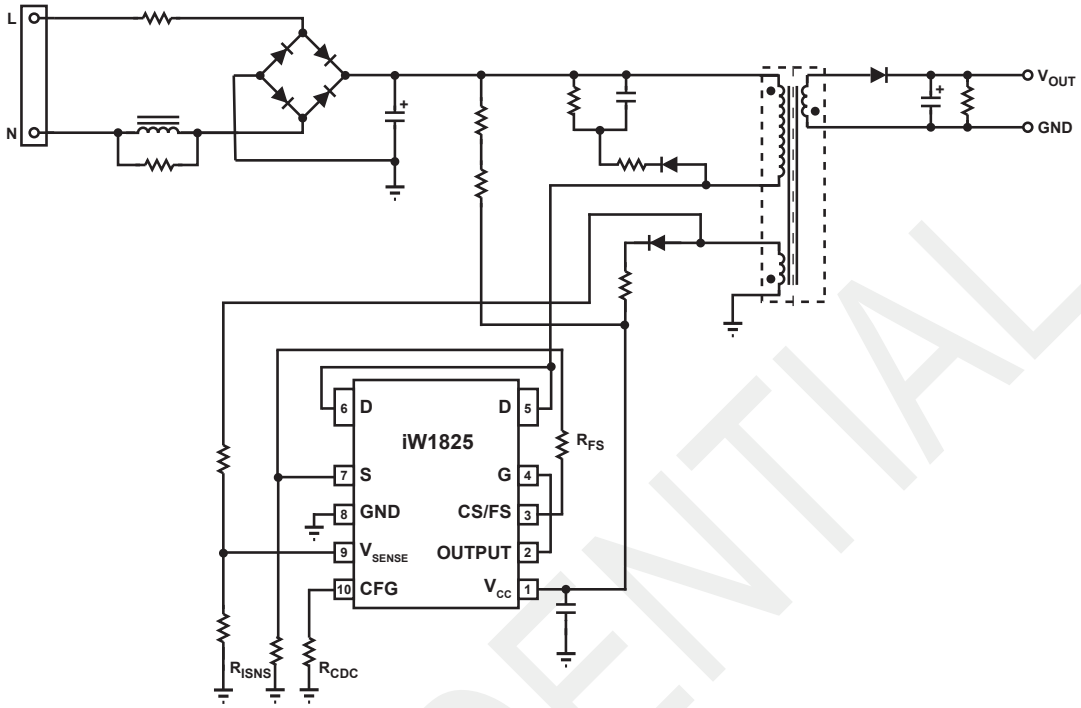


Figure 3.1 : iW1825 Typical Application Circuit
(Achieving < 75mW No-Load Power Consumption in 12V, 2A 24W Adapter Design).

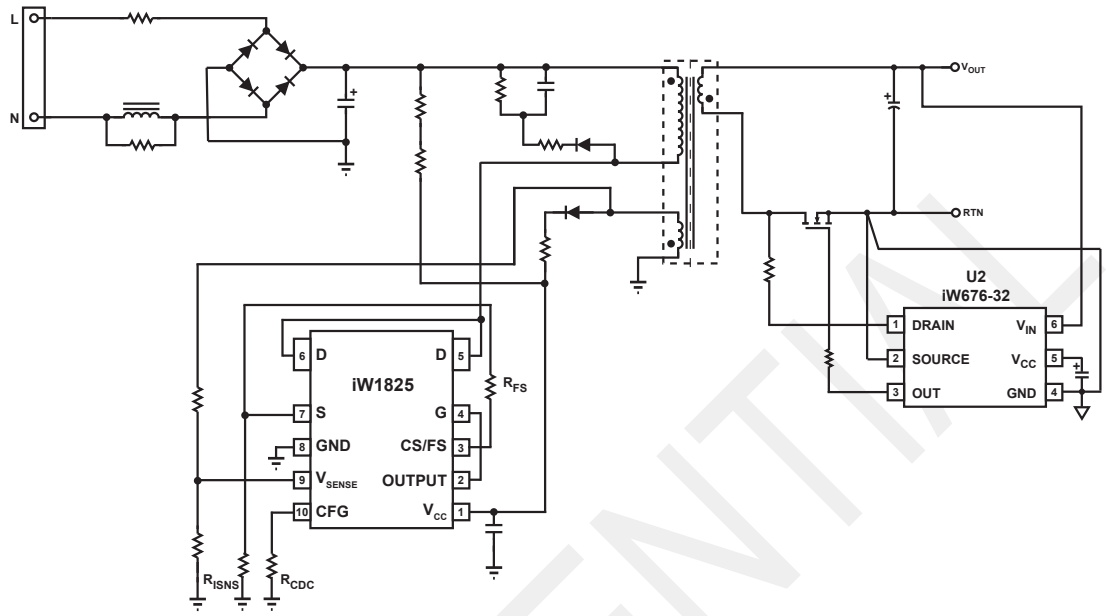


Figure 3.2 : iW1825 Typical Application Circuit with the iW676-32 Synchronous Rectifier Controller with Active Voltage Positioning Technology

WARNING:
The iW1825 is intended for high voltage AC/DC offline applications. Contact with live high voltage offline circuits or improper use of components may cause lethal or life threatening injuries or property damage. Only qualified professionals with safety training and proper precaution should operate with high voltage offline circuits.

iW1825 Output Power Table at Universal Input ($85V_{AC}$–$264V_{AC}$)

Condition	Open Frame[1]
Output Power (W)[2]	25

Notes:

Note 1. Maximum practical continuous output power measured at open frame ambient temperature of 50°C while minimum bulk capacitor voltage is kept above 90V (test unit is placed in a non-ventilated environment).

Note 2. The output power can vary depending on the power supply system designs and operating conditions.

4 Pinout Description

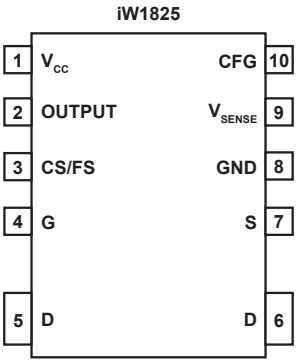


Figure 4.1 : 10-Lead SOIC Package

Pin Number	Pin Name	Type	Pin Description
1	V_{CC}	Power Input	IC power supply.
2	OUTPUT	Output	Gate drive for the MOSFET switch.
3	CS/FS	Analog Input	Primary-side current sense and minimum switching frequency configuration. It is used for cycle-by-cycle peak-current control and limit in primary-side CV/CC regulation. It is also used for minimum switching frequency configuration.
4	G	Analog Input	Gate of internal MOSFET. Connect to OUTPUT pin for proper operation.
5	D	Analog Input	Drain of internal MOSFET.
6	D	Analog Input	Drain of internal MOSFET.
7	S	Analog Input	Source of internal MOSFET.
8	GND	Ground	Ground.
9	V_{SENSE}	Analog Input	Auxiliary voltage sense. It is used for primary-side regulation and detection of secondary-side load transient signal.
10	CFG	Analog Input	In iW1825-01 and iW1825-31 options, it is used for external cable drop compensation (CDC) configuration and supplemental output over-voltage protection (OVP). In the iW1825-10 option, it is dedicated to input OVP.

5 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded.

Parameter	Symbol	Value	Units
DC supply voltage range (pin 1, I_{CC} = 20mA max)	V_{CC}	-0.3 to 25.0	V
Continuous DC supply current at V_{CC} pin (V_{CC} = 15V)	I_{CC}	20	mA
OUTPUT (pin 2)		-0.3 to 20.0	V
V_{SENSE} input (pin 9, I_{VSENSE} ≤ 10mA)		-0.7 to 4.0	V
CS/FS input (pin 3)		-0.3 to 4.0	V
CFG (pin 10, I_{CFG} ≤ 20mA)		-0.8 to 4.0	V
Drain-source voltage	V_{DSS}	700	V
Single Pulse Avalanche Energy (starting T_J = 25°C)	E_{AS}	60	mJ
Maximum junction temperature	T_{JMAX}	150	°C
Operating junction temperature	T_{JOPT}	-40 to 150	°C
Storage temperature	T_{STG}	-65 to 150	°C
ESD rating per JEDEC JS-001-2017		±2,000	V
Latch-up test per JESD78E		±100	mA

Notes:

Note 1. Repetitive rating; pulse width limited by maximum junction temperature.

6 Thermal Characteristics

Parameter	Symbol	Value	Units
Thermal Resistance Junction-to-Ambient[1]	θ_{JA}	55.6	°C/W
Thermal Resistance Junction-to-Drain pin (pin 5 and pin 6)[2]	ψ_{JB}	31.1	°C/W
Thermal Shutdown Threshold[3]	T_{SD}	150	°C
Thermal Shutdown Recovery[3]	T_{SD-R}	120	°C

Notes:

Note 1. Device is mounted on a JEDEC single-sided board with 83mm^2 of 70µm thick copper, in a one-cubic-foot natural convection chamber with 1W dissipated power.

Note 2. ψ_{JB} [Psi Junction to Board] provides an estimation of the die junction temperature relative to the PCB [Board] surface temperature. ψ_{JB} is measured at the ground pin (pin 8) without using any thermal adhesives. See Section 10.14 for more information.

Note 3. These parameters are typical and they are guaranteed by design.

7 Electrical Characteristics

V_{CC} = 12V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{SENSE} SECTION (Pin 9)						
Input leakage current	I_{BVS}	V_{SENSE} = 2V			1	µA
Nominal voltage threshold	$V_{SENSE(NOM)}$	T_A = 25°C, negative edge	1.521	1.536	1.551	V
V_{SENSE}-based output OVP threshold with no CDC compensation (Note 1)	$V_{SENSE(MAX)}$	T_A = 25°C, negative edge	1.742	1.838	1.926	V
CS/FS SECTION (Pin 3)						
Over-current threshold	V_{OCP}		1.11	1.15	1.19	V
CS/FS regulation upper limit (Note 2)	$V_{IPK(HIGH)}$			1.00		V
CS/FS regulation lower limit (Note 2) (Note 3)	$V_{IPK(LOW\_kHz)}$	R_{FS} < 0.65k or R_{FS} > 1.95k		0.23		V
CS/FS regulation lower limit (Note 2) (Note 3)	$V_{IPK(LOW\_Hz)}$	1.05k < R_{FS} < 1.35k		0.28		V
Input leakage current	I_{LK}	CS/FS = 1.0V			1	µA
CFG SECTION (Pin 10)						
OVP shutdown threshold (rising edge)	$V_{SD-TH(R)}$		1.75	1.8	1.85	V
OVP recovery hysteresis	$V_{SD-HYS(R)}$		3	12	24	mV
OUTPUT SECTION (Pin 2)						
Driver pull-down ON-resistance	$R_{DS(ON)PD}$	I_{SINK} = 5mA	5	9.6	15	Ω
Driver pull-up ON-resistance	$R_{DS(ON)PU}$	I_{SOURCE} = 5mA	65	75	90	Ω
Rise time (Note 2)	t_R	T_A = 25°C, C_L = 330pF 10% to 90%		95		ns
Fall time (Note 2)	t_F	T_A = 25°C, C_L = 330pF 90% to 10%		14		ns
Maximum switching frequency (Note 2) (Note 4)	f_{SW_MAX}	> 50% load		79		kHz
Minimum switching frequency (Note 2) (Note 3)	f_{SW_MIN}	1.05k < R_{FS} < 1.35k		0.14		kHz

6 Electrical Characteristics (cont.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{CC} SECTION (Pin 1)						
Recommended operating voltage range (Note 2)	V_{CC}				18	V
Pre-start-up threshold	$V_{CC(PRE\_ST)}$	V_{CC} rising	11	12	14.5	V
Start-up threshold	$V_{CC(ST)}$	V_{CC} rising	12.7	13.7	14.7	V
Under-voltage lockout threshold	$V_{CC(UVL)}$	V_{CC} falling	6.1	6.4	6.7	V
Latch release threshold	$V_{CC(RLS)}$	V_{CC} falling	3.8	4.5	5	V
V_{CC} over-voltage protection level	$V_{CC(OVP)}$	V_{CC} rising	21	23	24	V
Start-up current (Note 2)	$I_{IN(ST)}$	V_{CC} = 8V		1		µA
Start-up current level 2	$I_{IN(ST2)}$	$V_{CC(PRE\_ST)} < V_{CC} < V_{CC(ST)}$		10	12.5	µA
Quiescent current	I_{CCQ}	100pF at OUTPUT, V_{SENSE} = 1.4V	1.8	2.6	3.3	mA
Quiescent current, low power mode, Adapter	$I_{CC\_NL\_AD}$		0.1	0.22	0.35	mA
MOSFET SECTION (Pin 4, 5, 6 and 7)						
Drain-source break-down voltage	BV_{DSS}	V_{GS} = 0V, I_D = 0.25mA	700			V
Static drain-source on-resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 1.0A		1.05	1.4	Ω
Drain-source leakage current	I_{DSS}	V_{DS} = 700V, V_{GS} = 0V			1	µA
THERMAL CHARACTERISTICS						
Thermal shutdown threshold (Note 2)	T_{SD}			140		°C
Thermal shutdown hysteresis (Note 2)	T_{SD_HYS}			20		°C
Thermal shutdown recovery (Note 2)	T_{SD_R}			120		°C
V_{AUX} Open Protection						
V_{AUX} open detection threshold (iW1825-01 and iW1825-31 only)	V_{AUX_OPEN}		20	40	70	mV

Notes:

Note 1. The V_{SENSE}-based output OVP threshold depends on the CDC setup, see Section 10.14 for more details.

Note 2. These parameters are not 100% tested. They are guaranteed by design and characterization.

Note 3. The minimum switching frequency and the CS/FS regulation lower limit are user-configurable by the resistor connected to the CS/FS pin. Refer to Section 10.6 for details.

Note 4. Operating frequency varies based on the load conditions, see Section 10.6 for more details.

8 Typical Performance Characteristics

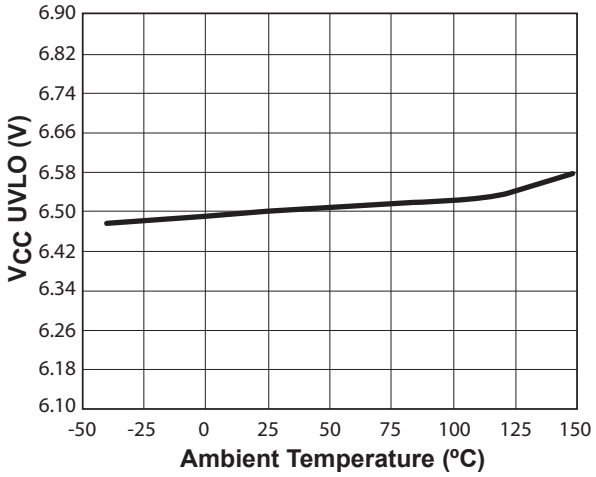


Figure 8.1 : V_{CC} UVLO vs. Temperature

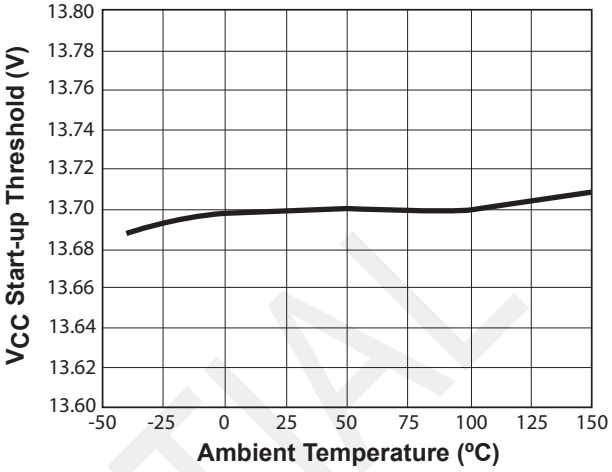


Figure 8.2 : Start-up Threshold vs. Temperature

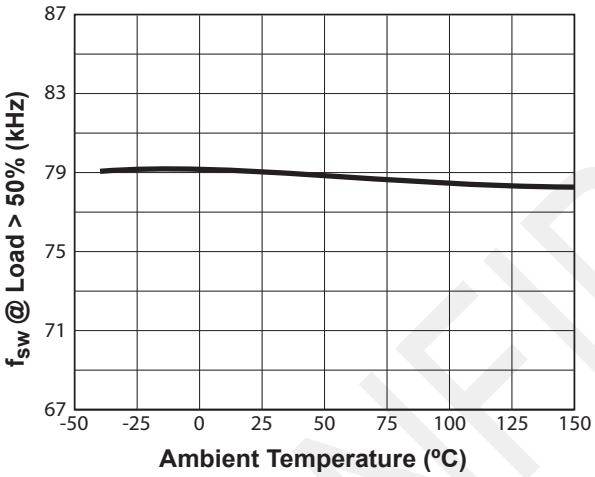


Figure 8.3 : Switching Frequency vs. Temperature[1]

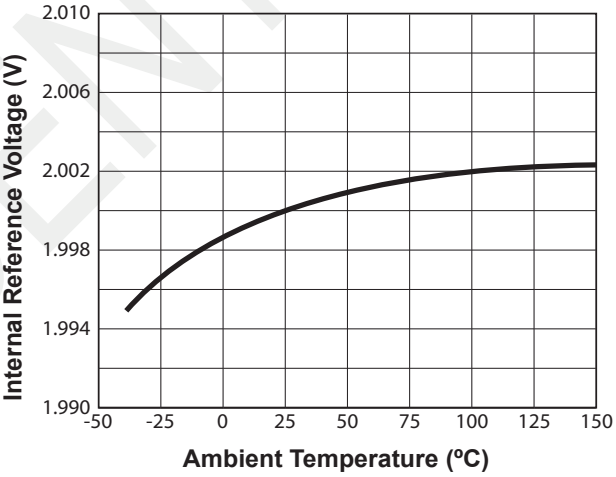


Figure 8.4 : Internal Reference vs. Temperature

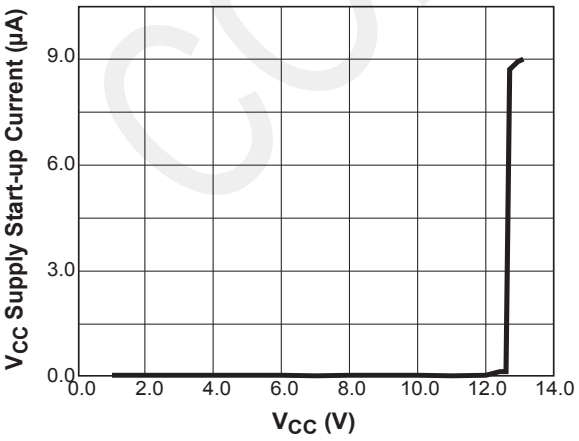


Figure 8.5 : V_{CC} Supply Start-up Current vs. V_{CC}

Note: Operating frequency varies based on the load conditions, see Section 10.6 for more details.

9 Functional Block Diagram

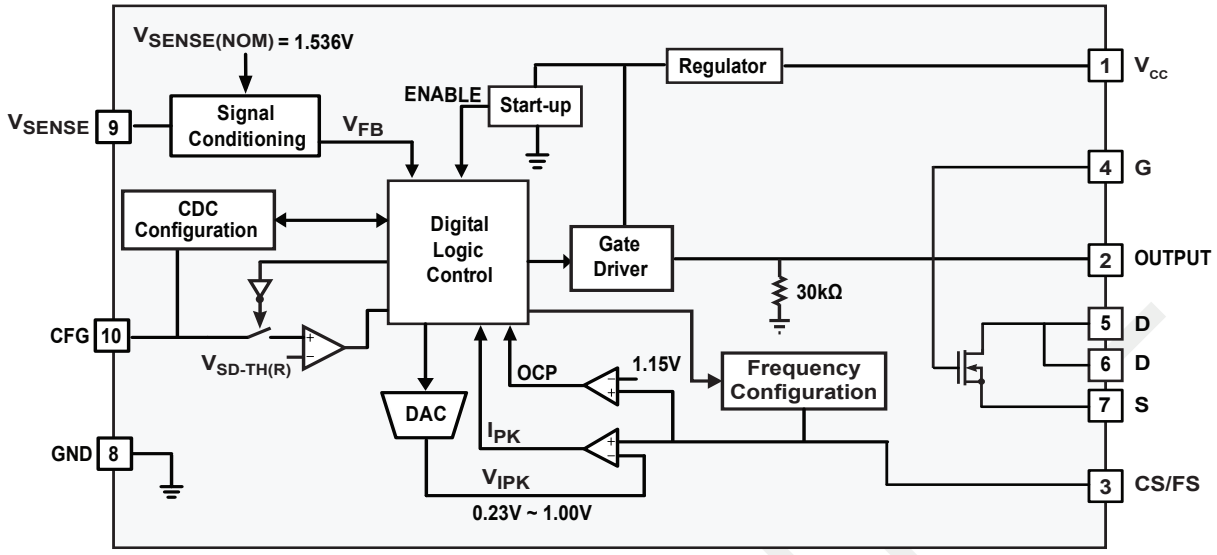


Figure 9.1 : iW1825 Functional Block Diagram

Note: CDC configuration is disabled in the iW1825-10 option.

10 Theory of Operation

The iW1825 is a digital controller which uses a new, proprietary primary-side control technology to eliminate the opto-isolated feedback and secondary regulation circuits required in traditional designs. This results in a low-cost solution for low power AC/DC adapters. The core PWM processor uses fixed-frequency Discontinuous Conduction Mode (DCM) operation at higher power levels and switches to variable frequency operation at light loads to maximize efficiency. Furthermore, Dialog's digital control technology enables fast dynamic response, tight output regulation, and full-featured circuit protection with primary-side control.

The block diagram in Figure 10.1 illustrates the iW1825 operating in peak current mode control. The digital logic control block generates the switching on-time and off-time information based on the output voltage and current feedback signal and provides commands to dynamically control the external MOSFET gate voltage. The CS/FS is an analog input configured to sense the primary current in a voltage form. In order to achieve the peak current mode control and cycle-by-cycle current limit, the V_{IPK} sets the threshold for the CS/FS to compare with, and it varies in the range of 0.23V (typical) to 1.00V (typical) under different line and load conditions. The system loop is automatically compensated internally by a digital error amplifier. Adequate system phase margin and gain margin are guaranteed by design and no external analog components are required for loop compensation. The iW1825 uses an advanced digital control algorithm to reduce system design time and increase reliability.

Furthermore, accurate secondary constant current operation is achieved without the need for any secondary-side sense and control circuits.

The iW1825 uses adaptive multi-mode PWM/PFM control to dynamically change the MOSFET switching frequency for efficiency, EMI, and power consumption optimization. In addition, it achieves unique MOSFET quasi-resonant switching to further improve efficiency and reduce EMI. Built-in single-point fault protection features include over-voltage protection (OVP), output short-circuit protection (SCP), over-current protection (OCP), and CS/FS fault detection. When the no-load switching frequency is configured at 1.8kHz, the iW1825 can achieve 75mW no-load power consumption with fast dynamic load response.

Dialog's digital control scheme is specifically designed to address the challenges and trade-offs of power conversion design. This innovative technology is ideal for balancing new regulatory requirements for green mode operation with more practical design considerations such as minimum cost, smallest size, and high performance output control.

10.1 Pin Detail

Pin 1 – V_{CC}

Power supply for the controller during normal operation. The controller starts up when V_{CC} reaches 13.7V (typical), and shuts down when the V_{CC} voltage drops below 6.5V (typical). A decoupling capacitor of 0.1µF or so should be connected between the V_{CC} pin and GND.

Pin 2 – OUTPUT

Gate drive for the external power MOSFET switch.

Pin 3 – CS/FS

Primary current sense and minimum switching frequency setting. Used for cycle-by-cycle peak current control and limit. It is also used to configure the minimum switching frequency at the beginning of start-up.

Pin 4 - G

Gate of the internal MOSFET. Must be connected to pin 2 for proper operation.

Pin 5 and Pin 6 – D

Drain pins of the internal MOSFET.

Pin 7 – S

Source of the internal power MOSFET.

Pin 8 – GND

Ground.

Pin 9 – V_{SENSE}

Sense signal input from auxiliary winding. This provides the secondary voltage feedback used for output regulation.

Pin 10 – CFG

In the iW1825-01 and iW1825-31, it is used to configure external cable drop compensation (CDC) at the beginning of start-up and provide output over-voltage protection during normal operation by sensing output voltage via the auxiliary winding. In iW1825-10, it is used to provide input over-voltage protection by sensing the input voltage directly or via an extra winding.

10.2 Start-Up and Soft-Start

Prior to start-up, the ENABLE signal is low, as shown in Figure 10.1. The voltage on the input high voltage capacitor provides start-up current to charge the V_{CC} bypass capacitor. When the V_{CC} bypass capacitor is charged to a voltage higher than the start-up threshold $V_{CC(ST)}$, the ENABLE signal becomes active and the iW1825 begins to perform the initial OTP check (see Section 9.16), followed by auxiliary winding open detection, CDC configuration (see Section 10.12) and LOM configuration (see Section 10.6). Afterwards, the iW1825 commences the soft-start function. During this start-up process an adaptive soft-start control algorithm is applied, where the initial output pulses are small and gradually get larger until the full pulse width is achieved. The peak current is limited cycle by cycle by the I_{PEAK} comparator. If at any time the V_{CC} voltage drops below the under-voltage lockout (UVLO) threshold $V_{CC(UVL)}$, the

iW1825 goes to shutdown. At this time the ENABLE signal becomes low and the V_{CC} capacitor begins to charge up again towards the start-up threshold to initiate a new soft-start process.

In the iW1825-10, the input over-voltage protection is enabled after the initial OTP check.

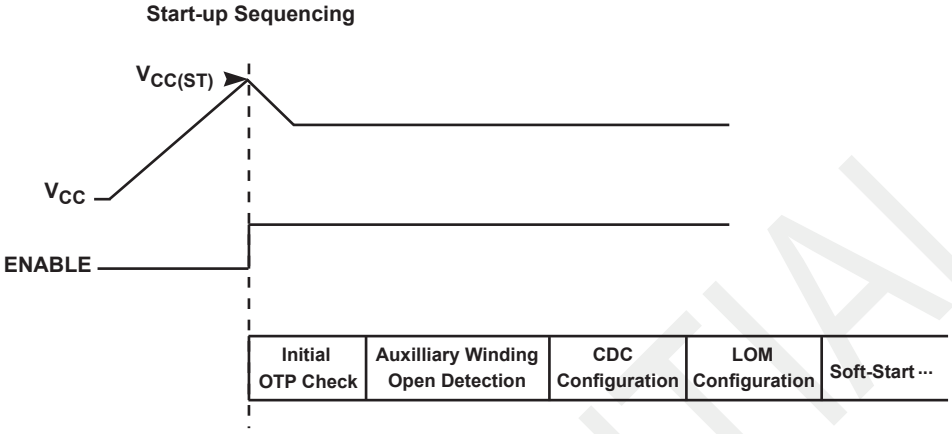


Figure 10.1 : Start-up Sequencing Diagram
(iW1825-10 - Auxiliary Winding Open Detection and CDC Configuration are Disabled)

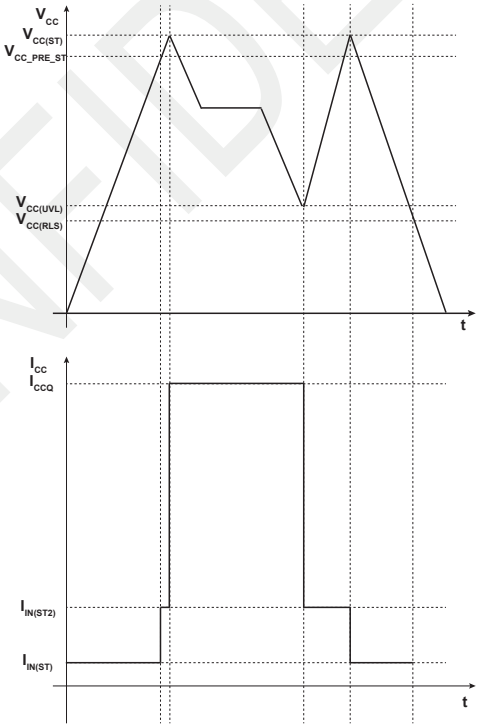


Figure 10.2 : Start-up Current

Figure 10.2 shows the I_{CC} current levels at different states. Before the start-up, the voltage at V_{CC} is zero. When input voltage is applied, it provides start-up current to charge the V_{CC} bypass capacitor. The current during this start-up state, noted as $I_{IN(ST)}$ in Figure 10.2, is as low as 1uA. As soon as the voltage at V_{CC} reaches $V_{CC(PRE\_ST)}$, the current at V_{CC} increases to $I_{IN(ST2)}$. When the V_{CC} reaches the start-up threshold $V_{CC(ST)}$, the operation current of iW1825 becomes I_{CCQ}. The operation current varies with the system load and may drops to as low as 0.22mA if the system operates at low power mode.

During shut-down, the V_{CC} voltage drops. When V_{CC} reaches the under-voltage lockout threshold $V_{CC(UVL)}$, the current at V_{CC} drops to the level of $I_{IN(ST2)}$. If the V_{CC} continues to drop below the latch release threshold $V_{CC(RLS)}$, the current at V_{CC} further reduces to $I_{IN(ST)}$.

10.3 Understanding Primary Feedback

Figure 10.3 illustrates a simplified flyback converter. When the switch Q1 conducts during $t_{ON}(t)$, the current $i_g(t)$ is directly drawn from rectified $v_g(t)$. The energy $E_g(t)$ is stored in the magnetizing inductance L_M. The rectifying diode D1 is reversely-biased and the load current I_O is supplied by the secondary capacitor C_O. When Q1 turns off, D1 conducts and the stored energy $E_g(t)$ is delivered to the output.

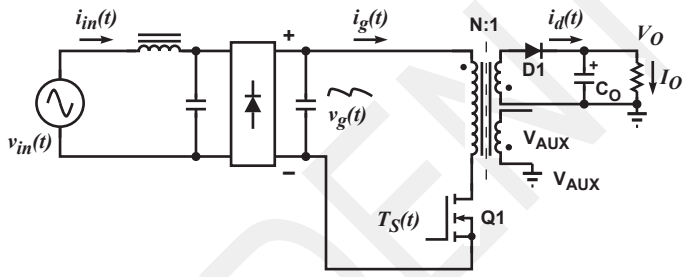


Figure 10.3 : Simplified Flyback Converter

In order to tightly regulate the output voltage, the information about the output voltage and load current must be accurately sensed. In the DCM flyback converter, this information can be read via the auxiliary winding or the primary magnetizing inductance (L_M). During the Q1 on-time, the load current is supplied from the output filter capacitor C_O. The voltage across L_M is $v_g(t)$, assuming the voltage dropped across Q1 is zero. The current in Q1 ramps up linearly at a rate of:

$$\frac{di_g(t)}{dt} = \frac{v_g(t)}{L_M} \qquad (10.1)$$

At the end of on-time, the current has ramped up to:

$$i_{g\_peak}(t) = \frac{v_g(t) \times t_{ON}}{L_M} \qquad (10.2)$$

This current represents a stored energy of:

$$E_g = \frac{L_M}{2} \times i_{g\_peak}(t)^2 \qquad (10.3)$$

When Q1 turns off at t_O, $i_g(t)$ in L_M forces a reversal of polarities on all windings. Ignoring the communication-time caused by the leakage inductance L_K at the instant of turn-off t_O, the primary current transfers to the secondary at a peak amplitude of:

$$i_d\ t = \frac{N_P}{N_S} \times i_{g\_peak}\ t \qquad (10.4)$$

Assuming the secondary winding is master, and the auxiliary winding is slave, the auxiliary voltage is given by:

$$V_{AUX} = \frac{N_{AUX}}{N_S}(V_O + \Delta V) \qquad (10.5)$$

and reflects the output voltage as shown in Figure 10.4.

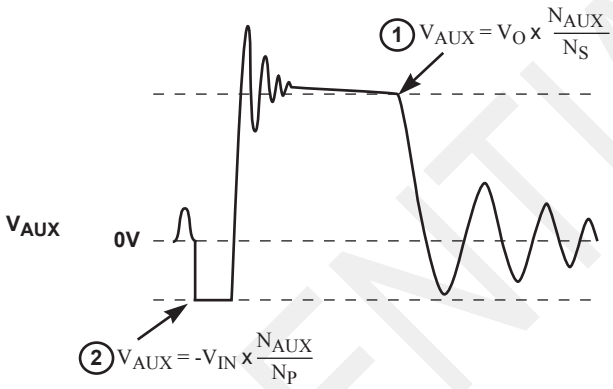


Figure 10.4 : Auxiliary Voltage Waveforms

The voltage at the load differs from the secondary voltage by a diode drop and IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage is a fixed ΔV. Furthermore, if the voltage can be read when the secondary current is small, ΔV is also small.

The real-time waveform analyzer in the iW1825 reads this information cycle by cycle. The device then generates a feedback voltage V_{FB}. The V_{FB} signal precisely represents the output voltage under most conditions and is used to regulate the output voltage.

10.4 Constant Voltage Operation

After soft-start has been completed, the digital control block measures the output conditions. It determines output power levels and adjusts the control system according to a light load or heavy load. If this is in the normal range, the device operates in the Constant Voltage (CV) mode, and changes the pulse width (t_{ON}) and off time (t_{OFF}) in order to meet the output voltage regulation requirements.

If no voltage is detected on V_{SENSE} it is assumed that the auxiliary winding of the transformer is either open or shorted and the iW1825 shuts down.

10.5 Current Limit and Constant Current Operation

In overload condition, the iW1825 enters constant current (CC) mode to limit the output current on a cycle-by-cycle basis. In this mode of operation the output current is limited to a constant level regardless of the output voltage, while avoiding continuous conduction mode operation. In case of very heavy loading when the output voltage is low enough, the iW1825 shuts down.

The iW1825 senses the load current indirectly through the primary current, which is detected by the pin CS/FS through a resistor from the MOSFET source to ground.

When operating in the CC mode, with the decrease of equivalent load resistance or battery voltage, both the output voltage and V_{CC} decrease. After the V_{CC} voltage is below UVLO threshold the iW1825 shuts down (see Section 10.11). Meanwhile, the iW1825 monitors the output voltage, and shuts down the system when the detected output voltage is lower than certain level; this is known as “CC shutdown voltage.” The shutdown can occur under either one of the above two conditions.

The “CC shutdown voltage” here refers to the voltage at the cable end, and the output voltage at the PCB end is the sum of the “CC shutdown voltage” and the “Cable Comp” (specified in Section 10.13 – iW1825-01 and iW1825-31). The “CC shutdown voltage” is specified for a nominal 5V output voltage. For different output voltages, the actual “CC shutdown voltage” must be scaled accordingly. As a result, the “CC shutdown voltage” option can adaptively match the cable voltage drop at CC mode. For instance, for a 12V, 2A charger design, if the cable resistance is around 180mΩ, the voltage drop across the cable is around 360mV under both the CV mode full load and CC mode conditions. Assuming the 0.75V CC shutdown voltage option is used in the 12V, 2A charger design (scales to 1.8V by multiplying the 0.75V by the higher nominal output voltage – 12V – and dividing by 5V). If no CDC is configured, or available as is the case with the -10 option, the voltage at the PCB end is around 12V at full load and the voltage at the cable end is around 11.64V. As the current increases beyond the maximum load current and the circuit enters constant current mode, the output voltage will decrease until the voltage at the cable end decreases to 1.44V and the voltage at the PCB end decreases to 1.8V, at which point the CC shutdown occurs. Normally a CDC is needed in this design to achieve a desirable voltage regulation at CV mode, for example, the CDC is configured as 360mV. Then at CV full load, the voltage at the PCB end is around 12.36V, and the voltage at the cable end is around 12V. Correspondingly the CC shutdown occurs when the voltage at the PCB end decreases to 2.16V, and the voltage at the cable end decreases to 1.8V.

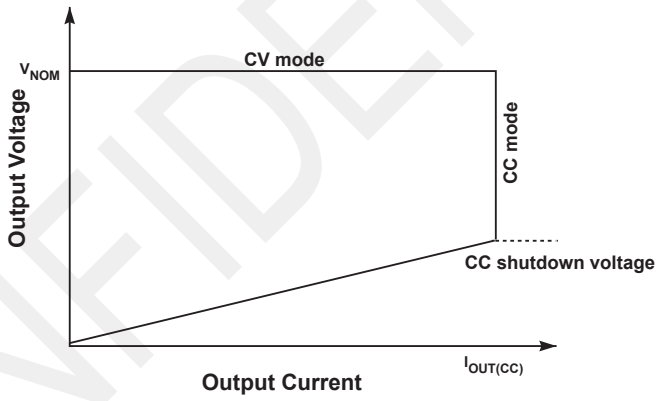


Figure 10.5 : Power Envelope

10.6 Multi-Mode PWM/PFM Control and Quasi-Resonant Switching, and User-Configurable Light-Load Modes (LOM)

The iW1825 uses a proprietary adaptive multi-mode PWM/PFM control to dramatically improve the light-load efficiency and the overall average efficiency. The operating mode changes as the load decreases in order to maximize efficiency. Figure 10.6 shows how the switching frequency and the V_{IPK} vary with the load. During constant voltage (CV) mode operation under heavy load, the iW1825 operates in pulse-width-modulation (PWM) mode. In PWM mode, the switching frequency remains approximately constant. As the output load decreases, the on-time (t_{ON}) decreases, and the controller adaptively transitions to a pulse-frequency-modulation (PFM) mode. In PFM mode, the MOSFET is turned on for a set duration under a given instantly-rectified AC input voltage, but its off-time is modulated by the load current, decreasing the switching frequency.

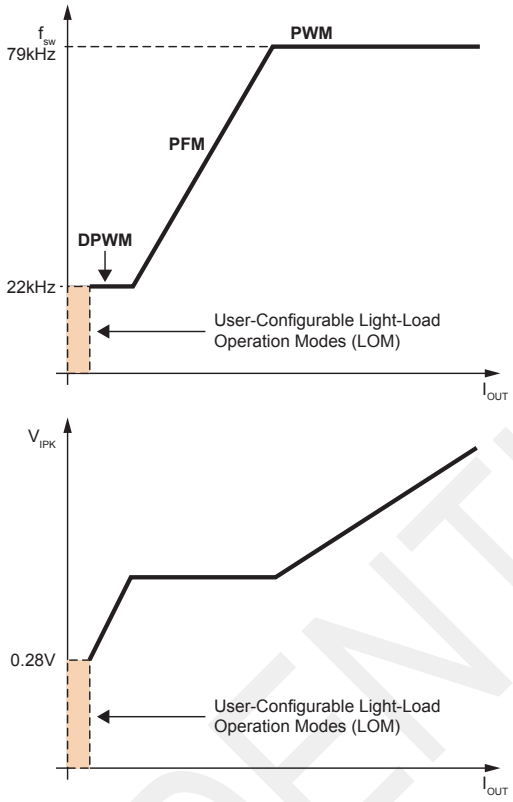


Figure 10.6 : Multi-Mode PWM/PFM in iW1825 at Mid-High Loads

When the switching frequency approaches the human ear audio band, the iW1825 transitions to a second level of PWM mode, namely the Deep PWM mode (DPWM). In the DPWM mode, the switching frequency stays approximately 22kHz in order to avoid audible noise. As the load current continues to decrease, the iW1825 transitions to Deep PFM mode (DPFM), which reduces the switching frequency to a very low level. Although the switching frequency drops across the audible frequency range during the DPFM mode, the output current in the power converter has reduced to an insignificant level and therefore, the power converter practically produces no audible noise.

The iW1825 allows the user to configure the operation mode of the system at light/no load according to the system requirements in order to minimize the overall system cost. This light-load operation mode (LOM) configuration is only performed once during start-up. It is completed after the CDC configuration but before soft-start commences. During the LOM configuration, the internal digital control block senses the total external resistance value between the CS/FS pin and ground, and then sets a corresponding LOM. Figure 3.1 shows a simple circuit to set the LOM by connecting a resistor, R_{FS}, directly to the CS/FS pin. The R_{FS} resistor combined with the R_{ISNS} value creates the total resistance used to program the LOM. Figures 10.7 and 10.8 show how the switching frequency and V_{IPK} vary with load in different LOM settings.

Table 10.1 shows the resistance range for each of the four LOM settings. In practice, it is recommended to select resistance values in the middle of the range wherever possible. Resistor variation should be taken into consideration to ensure the correct setting.

LOM #	R_{FS}+ R_{ISNS} Range (kΩ)		DDPWM Mode Switching Frequency (f_{sw_DDPWM}) (kHz)	Minimum Switching Frequency (f_{SW_MIN}) (kHz)	Secondary-Side Active Voltage Positioning Support	Primary Peak Current Regulation Voltage (V_{IPK}) at DPFM (V)
	Min	Max				
1	0	0.65	1.8	1.62	No	0.23
2	1.05	1.35	No DDPWM mode	0.14	Yes	0.28
3	1.95	2.86	2.7	2.43	No	0.23
4	3.7	6	4	3.6	No	0.23

Table 10.1: Recommended Resistance Range for Different Light-Load Operating Modes (LOM) and Their Corresponding Primary Peak Current Regulation Voltage

If the design requires very low no-load power consumption (< 50mW), LOM #2 should be chosen for 140Hz minimum switching frequency operation (Figure 10.7). In this LOM setting, the switching frequency in DPFM continues to drop as the load current reduces until the switching frequency reaches 140Hz. The primary peak current regulation voltage (V_{IPK}) in DPFM mode is set at 0.28V. The primary switch turns off when the voltage on the CS/FS pin reaches this level. To achieve the best dynamic load response (DLR), a secondary-side IC with active voltage positioning, such as the iW676-3X, is recommended when the iW1825 is configured for this mode.

If the application can tolerate higher no-load power consumption (75mW or above), the device can be configured in LOM #1, 3 or 4 (Figure 10.8) to maintain relatively high no-load switching frequency for fast dynamic load response. In these modes, the primary peak current regulation voltage in the DPFM mode is set at 0.23V (Figure 10.8). As the load current reduces to very light load or no-load condition, the iW1825 transitions from the DPFM to the third level of PWM mode, namely Deep-Deep PWM mode (DDPWM), in which the switching frequency is fixed at 1.8kHz, 2.7kHz, or 4kHz depending on the resistance set at the CS/FS pin. The primary on-time is reduced in DDPWM to reduce the energy delivered to the secondary side.

As the load further decreases, the primary on-time is reduced to minimum in DDPWM mode. The iW1825 transitions to a third level of PFM mode, namely the Deep-Deep PFM Mode (DDPFM). In this mode, the switching frequency decreases as the load decrease. The minimum switching frequency is clamped at 90% of the DDPWM mode switching frequency.

The typical no-load operation point of the system is recommended to be in the middle of the DDPWM mode, as shown in Figure 10.8. The DDPFM mode is designed to provide additional margin of output voltage regulation at no load considering the variation of the system parameters.

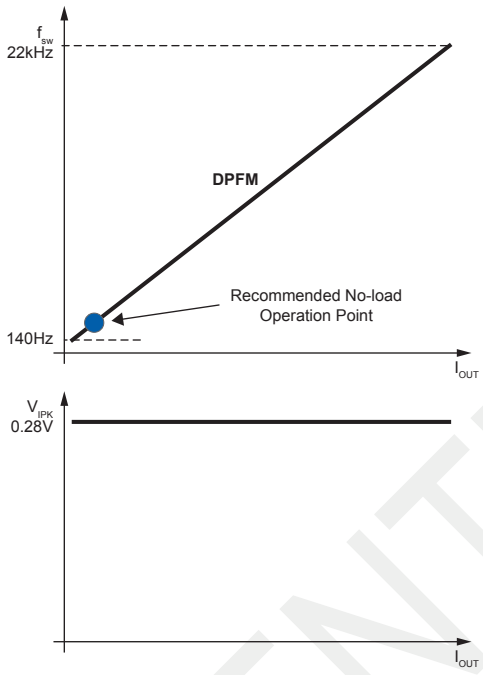


Figure 10.7 : Light-Load Operation Mode (LOM) #2

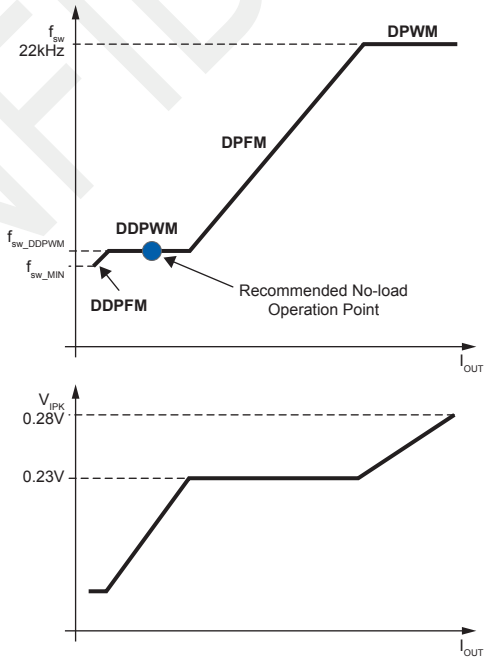


Figure 10.8 : Light-Load Operation Mode (LOM) #1, 3, or 4

10.7 Less Than 75mW No-Load Power and Fast Load Transient Response

The iW1825 features a distinctive DDPWM control in no-load conditions to help achieve low no-load power consumption and fast dynamic load response. With a 1.8kHz f_{SW_DDPWM}, the system no-load power can be less than 75mW for a typical 12V, 2A 24W application. The power supply system designs including the pre-load resistor selection should ensure the power supply can operate in the DDPWM mode under steady-state no-load condition. If the pre-load resistor is too small, the no-load power consumption increases; on the other hand, if it is too large, the output voltage may increase and even cause over-voltage since the switching frequency is fixed at a minimum 1.62kHz level.

While achieving ultra-low no-load power consumption, the iW1825 implements innovative proprietary digital control technology to intelligently detect any load transient events, and achieve fast dynamic load response for both one-time and repetitive load transients.

The most stringent dynamic load transient requirement is the no-load to load transient. The output voltage drop (cable-drop not included) ΔV_{OUT} is a function of the no-load switching frequency (f_{sw_DDPWM}), output capacitance (C_{OUT}) and the load applied (I_{OUT_STEP}), as shown in Equation 10.6.

$$\Delta V_{OUT} = \frac{I_{OUT\_STEP}}{f_{SW\_DDPWM} \times C_{OUT}} + 0.1V \qquad (10.6)$$

If the system requirement specifies the maximum output voltage drop (ΔV_{OUT_MAX}) from the nominal output voltage (V_{OUT_NOM}) during no-load to I_{OUT_STEP} load change, the minimum output capacitance (C_{OUT_MIN}) required to meet the specification can be calculated with Equation 10.7.

$$C_{OUT\_MIN} = \frac{I_{OUT\_STEP}}{f_{SW\_DDPWM} \times (\Delta V_{OUT\_MAX} + 0.1V)} \qquad (10.7)$$

10.8 Lower No-Load Power Consumption with Secondary Active Voltage Positioning

When the iW1825 is configured with the minimum switching frequency of 140Hz, the power consumption reduces to a minimal level, but the very low switching frequency can cause diminished transient response time. When used with a secondary-side controller with active voltage positioning such as the iW676-3X, a power supply with lower no-load power consumption and fast transient response can be achieved.

In this configuration, the iW1825 is operating in the DPFM mode at no load where the switching frequency can drop to as low as 140Hz and still maintain a tight closed-loop control of the output voltage. The distinctive DPFM operation allows the use of a relatively large pre-load resistor which helps to reduce the no-load power consumption. In the meantime, the iW1825 implements an intelligent low-power management technique that achieves ultra-low operating current (as low as 220µA) at no-load.

When a load transient event from a light load to a heavy load happens, the output voltage drops. When such a transient event occurs, the secondary-side active voltage positioning controller injects a pulse of current into the transformer. The pulse current induces ringing on the auxiliary winding and this ringing is detected by the iW1825. After the iW1825 detects this signal, it can intelligently confirm if this signal is caused by an undershoot event and distinguish it from noise, and then it promptly increases the switching frequency and the t_{ON} to deliver more power to the secondary side in order to bring the output voltage back to regulation.

When the iW1825 is configured in LOM #2, the CFG-Pin based Supplemental Output OVP (Section 10.15) should be implemented to provide additional over-voltage protection in case noise mis-triggers the undershoot event. Furthermore, a resistor is recommended in parallel with the auxiliary winding to provide damping of the ringing when necessary.

10.9 Variable Frequency Operation Mode

In each of the switching cycles, the falling edge of V_{SENSE} is checked. If the falling edge of V_{SENSE} is not detected, the off-time is extended until the falling edge of V_{SENSE} is detected. The maximum allowed transformer reset time is 110µs. When the transformer reset time reaches 110µs, the iW1825 shuts off.

10.10 Internal Loop Compensation

The iW1825 incorporates an internal Digital Error Amplifier with no requirement for external loop compensation. For a typical power supply design, the loop stability is guaranteed to provide at least 45 degrees of phase margin and -20dB of gain margin.

10.11 Voltage Protection Features

The secondary maximum output DC voltage is limited by the iW1825. When the V_{SENSE} signal exceeds the output OVP threshold at point 1 indicated in Figure 10.3, the iW1825 shuts down.

For this V_{SENSE}-based OVP, latch function is available by product options given in Section 11.

The iW1825 uses an innovative proprietary digital control method to detect and analyze the switch ON time, which provides real-time indirect sensing and monitoring of the magnitude and shape of the DC bulk capacitor voltage. This enables the iW1825 to determine and distinguish various conditions of the AC input voltage such as brown-out, brown-in and unplug, and to take appropriate actions. When the AC input voltage drops to below normal operation range and the power supply input is still connected to the AC source, the iW1825 initiates brown-out protection and shuts down the power supply adaptively according to the power supply load condition. Meanwhile, a brown-in input voltage threshold is set with hysteresis. In the case of the power supply input being unplugged or disconnected from the AC source, the iW1825 continues to control the switching actions to discharge the DC bulk capacitor voltage to a safe level before shutting down the power supply.

Also, the iW1825 monitors the voltage on the V_{CC} pin, and the IC shuts down immediately when the voltage on this pin is below the UVLO threshold. The iW1825 also has a V_{CC} over-voltage protection (V_{CC} OVP). During an abnormal event, if the V_{CC} voltage is higher than the protection threshold, the switching is stopped and the iW1825 shuts down.

When any of these faults are met the IC remains biased to discharge the V_{CC} supply. Once V_{CC} drops below UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting start-up until the fault condition is removed. For the latched OVP version, the controller can only start up when the fault is removed and input is unplugged to allow V_{CC} to drop to 2.0V below the UVLO threshold.

10.12 PCL, OCP and SRS Protection

Peak-current limit (PCL), over-current protection (OCP) and sense-resistor-short protection (SRSP) are features built into the iW1825. With the CS/FS pin the iW1825 is able to monitor the peak primary current. This allows for cycle-by-cycle peak current control and limit. When the peak primary current multiplied by the current sensing resistor (R_{ISNS} in Figure 3.1) is greater than 1.15V, over-current is detected and the IC immediately turns off the gate driver until the next cycle. The output driver sends out a switching pulse in the following cycle, and the switching pulse continues if the OCP threshold is not reached; or, the switching pulse turns off again if the OCP threshold is reached. If the OCP occurs for several consecutive switching cycles, the iW1825 shuts down.

If the current sensing resistor R_{ISNS} is shorted prior to the power supply startup, there is a potential danger that an over-current condition may not be detected. Thus, the IC is designed to detect this sense-resistor-short fault during startup and the startup process is not pursued if the fault exists. The V_{CC} is discharged since the IC remains biased. Once the V_{CC} drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting to start up, but does not fully start up until the fault condition is removed.

10.13 CDC Configuration (Only Available on iW1825-01 and iW1825-31 Options)

The iW1825-01 and iW1825-31 incorporates an innovative approach to allow users to configure cable drop compensation (CDC) externally. This configuration is only performed once at the beginning of start-up. It is completed after the auxillary winding open detection check but before the LOM configuration. During the CDC configuration, the internal digital control block senses the external resistance value between the CFG pin and ground, and then sets a corresponding CDC level to allow the device to compensate for IR drop in the secondary circuitry during normal operation.

Figure 3.1 shows a simple circuit to set CDC level by connecting a resistor, R_{CDC}, from the CFG pin to ground. The iW1825-01 and iW1825-31 provides five levels of CDC configurations: 0mV, 180mV, 360mV, 720mV, and 1.08V, which refer to 12V nominal output voltage. Table 10.2 below shows the resistance range for each of the five CDC levels. In practice, it is recommended to select resistance in the middle of the range wherever possible.

The “Cable Comp” specified in Table 10.2 refers to the voltage increment at PCB end from no-load to operating current in the CC mode, with the assumption that the secondary diode voltage drop can be ignored at the point when the secondary voltage is sensed. Also, the “Cable Comp” is specified based on the nominal output voltage of 12V. For different output voltage, the actual voltage increment needs to be scaled accordingly.

To calculate the amount of cable compensation needed, take the resistance of the cable and connector and multiply it by the maximum output current.

For each of the CDC levels, the internal V_{SENSE}-based OVP thresholds are different. Table 10.2 also lists the typical OVP thresholds for each CDC level.

In iW1825-10, the CDC configuration is disabled. The CDC level is 0mV, disregarding the resistors at the CFG pin. And the corresponding OVP threshold is 1.838V.

R_{CDC} Range (kΩ)		Cable Comp (mV)	Output OVP Threshold (V)
Min	Max		
1.5	2.20	0	1.838
2.37	3.21	180	1.861
3.40	4.64	360	1.884
4.87	6.65	720	1.930
6.98	10	1080	1.976

Table 10.2: Recommended Resistance Range for Different CDC Levels and the Corresponding V_{SENSE}-Based Output OVP Threshold for 12V Output

10.14 External CFG-Based Supplemental Output OVP (iW1825-01 and iW1825-31)

The CFG pin can be used to provide external over-voltage protection (OVP) as well as external cable drop compensation (CDC) configuration. This external CFG-based OVP serves as a supplmental or extra protection in addition to the V_{SENSE}-based OVP. The circuit implementation can be found in Figure 10.9, where two resistors R1 and R2 form a voltage divider to sense output voltage via auxiliary winding, with the tapping point connected to the CFG pin. During the CDC configuration the iW1825-01 and iW1825-31 options do not send out any drive signal at the OUTPUT pin, and the switch Q1 remains in the off state. The resistors R1 and R2 are essentially connected in parallel since the auxiliary winding is virtually shorted. Consequently, the paralleled resistance of R1 and R2 sets the CDC level. Meanwhile, during normal operation, the CFG pin reflects the output voltage in real-time, in the similar fashion as the V_{SENSE} does at point 1 in Figure 10.4. The ratio of R1 to R2 sets the external OVP threshold.

The resistance values for the resistor divider, R1 and R2, can be derived as follows.

First, for the given CDC level, the paralleled resistance of R1 and R2 should be within the range listed in Table 10.2:

$$R_{CDC} = \frac{R_1 \times R_2}{R_1 + R_2} \qquad (10.8)$$

Second, during normal operation the voltage divider, R1 and R2, sets the desired OVP threshold:

$$\left(\frac{N_{AUX}}{N_{SEC}}\right) \times V_{OVP} \times \left(\frac{R_2}{R_2 + R_1}\right) >= V_{SD\text{-}TH(R)} \qquad (10.9)$$

where N_{AUX} is the number of turns for the auxiliary winding, N_{SEC} is the number of turns for the secondary winding, V_{OVP} is the desired OVP tripping point, and $V_{SD\text{-}TH(R)}$ is the internal comparator threshold (1.8V typically) for OVP detection.

The combination of Equations (10.8) and (10.9) leads to:

$$R_1 = \left(\frac{N_{AUX}}{N_{SEC}}\right) \times R_{CDC} \times \left(\frac{V_{OVP}}{V_{SD\text{-}TH(R)}}\right)$$

$$R_2 = \left(\frac{R_1}{R_1 - R_{CDC}}\right) \times R_{CDC} \qquad (10.10)$$

It is recommended the R_{CDC} value is taken as the median value of the resistance range as given in Table 10.2, and R1 and R2 can then be readily derived from Equation (10.10).

It should be noted when the CFG pin is used to provide external OVP, an additional constraint is applied to the resistance range given in Table 10.2. This is because for the OVP configuration in Figure 10.9, a large negative voltage may occur to the auxiliary winding (V_X in Figure 10.9) during the switch on-time, which can cause a negative current flowing out of the CFG pin. Care needs to be taken to ensure R1 and R2 are large enough, so that the resulting negative current is less than the maximum allowed current, specified in Section 5.

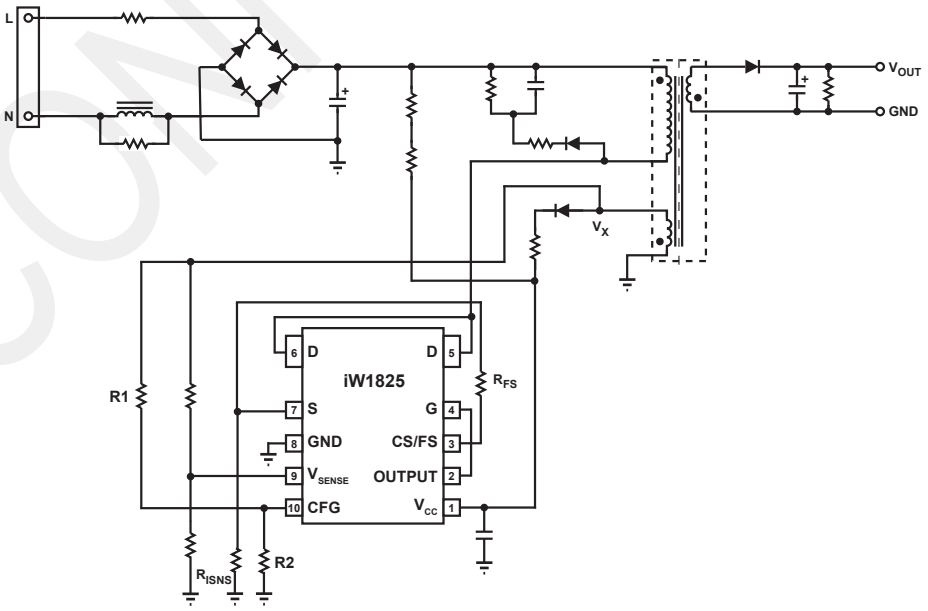


Figure 10.9 : Typical Application Circuit with CDC and CFG-Pin Based Supplemental Output OVP

10.15 External CFG-Based Input OVP (iW1825-10)

In iW1825-10, the CFG pin is used for input over-voltage protection, which is enabled after the initial OTP check during the start-up. The iW1825-10 continues to monitor the input voltage through a resistor divider. If the CFG pin voltage exceeds the threshold (1.8V typical) for 100µs, the iW1825-10 shuts down. An alternative method is to use an auxiliary winding on the transformer to monitor the input voltage. The advantage is lower loss compared to connecting a resistor divider to the high voltage input rail, with the disadvantage that the over-voltage protection doesn't begin until after switching starts.

10.16 Internal OTP

The iW1825 features an internal OTP which shuts down the device if the internal die junction temperature reaches above 140°C (typical). The device is kept off until the junction temperature drops below 120°C (typical), when the device initiates a new soft-start process to build up the output voltage.

10.17 Latch and Release

In the iW1825, the output OVP (including V_{SENSE}-based and the external CFG-based OVP) and CC shutdown can be latched (based on product option, see section 11). When the latch occurs, the device does not attempt to start again even with the fault cleared. In the latch state, the controller recycles itself by periodically ramping V_{CC} up and down between $V_{CC(ST)}$ and $V_{CC(UVL)}$, and the controller does not start up, provided the input stays connected to the AC source. To get out of the latch state, unplugging the input from the AC source is required, so that the V_{CC} is allowed to drop to 2.0V below $V_{CC(UVL)}$ to release the latch.

See section 12 to see options available with latched fault state.

10.18 SmartDefender™ Smart Hiccup Technology

In the traditional AC/DC adapter designs, once the control IC detects a fault and shuts down, there are two common ways to respond to a default:

(a) Shutdown and auto-restart—The switching pulses are sent out in every power-on-reset (POR) cycle after the V_{CC} reaches the startup threshold. In case of the USB cable short or partial short, this can have a high average output current from the USB and high average input power in the adapter, and it may generate excessive heat and cause damages. The auto-restart is commonly called "hiccup".

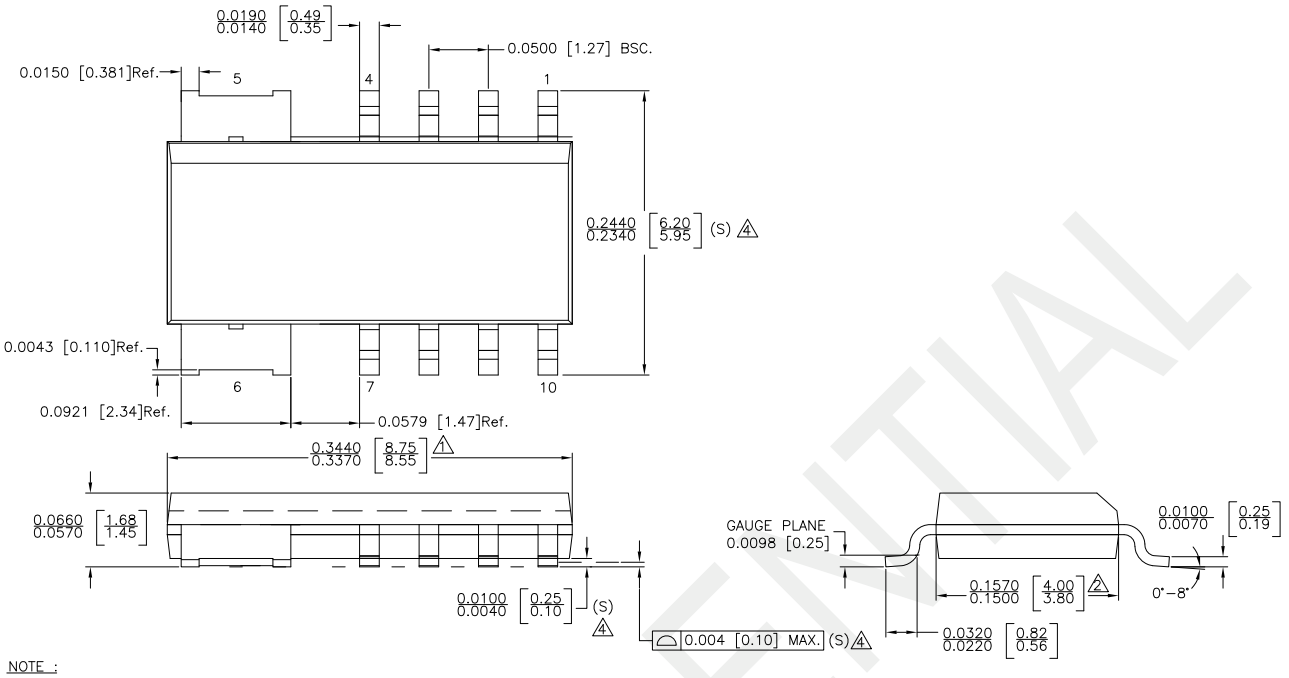
(b) Shutdown and latch—This normally requires the user to unplug the adapter from the AC input and recycle the power, which can create an inconvenient or bad experience.

To address this issue, the iW1825 implements Dialog's innovative and proprietary ***SmartDefender*** smart hiccup protection function (based on product option, see section 11). With ***SmartDefender*** technology, during the smart hiccup, the power supply only re-starts after a certain number of POR cycles (which means sending the switching pulses after V_{CC} reaches the startup threshold) instead of auto-restart in every POR cycle. In the iW1825 the ***SmartDefender*** function applies to the faults such as the output short and "CC shutdown," etc. Once these faults are detected, the iW1825 allows 2 cycles of auto-restart POR, and then blocks the next 6 cycles of auto-restart POR. This is equivalent to a 2/8 duty cycle. This operation mode continues until the faults are removed. In this way the ***SmartDefender*** technology effectively reduces the average output power at the fault conditions without latch.

10.19 iW1825 Product Options

In order to support a variety of applications with different system requirements, iW1825 provides several product options. Each product option may have different CC shutdown voltage etc. Please refer to the "Ordering Information" for detail.

11 Physical Dimensions



NOTE :

1. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 INCH PER SIDE.
2. DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 INCH PER SIDE.
3. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MS–012 AB.
4. LEAD SPAN/STAND OFF HEIGHT/COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERISTIC.(S)
5. CONTROL DIMENSIONS IN INECHES.[mm]

dialog SEMICONDUCTOR	
STATUS: RELEASED	SCALE: DO NOT SCALE
TERMINAL FINISH: NiPdAu (PPF)	
TITLE: 10 SOIC BATWING PACKAGE OUTLINE	
REV: A / REVISION NOTE: NEW DRAWING	DATE: 29–SEP–2015

12 Ordering Information

Part Number	Options[1]					Package	Description
	External CFG Over-Voltage Protection Option	CC Shutdown Voltage at 5V Output[2]	Latch Conditions	CDC	Smart Defender		
iW1825-01	Output	No CC Operation	Latch	Yes	No	SOIC-10	Tape & Reel[3]
iW1825-31	Output	0.75V	No Latch	Yes	Yes	SOIC-10	Tape & Reel[3]
iW1825-10	Input	4V	No Latch	No	Yes	SOIC-10	Tape & Reel[3]

Note 1: For availability of additional options, please contact Marketing.

Note 2: Please refer to section 10.5 for CC shutdown voltage at different nominal output voltages.

Note 3: Tape and reel packing quantity is 3,000/reel. Minimum packing quantity is 3,000.

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Contacting Dialog Semiconductor

United Kingdom (Headquarters)
Dialog Semiconductor (UK) LTD
Phone: +44 1793 757700

Germany
Dialog Semiconductor GmbH
Phone: +49 7021 805-0

The Netherlands
Dialog Semiconductor B.V.
Phone: +31 73 640 8822

Email
info_pcbg@diasemi.com

North America
Dialog Semiconductor Inc.
Phone: +1 408 845 8500

Japan
Dialog Semiconductor K. K.
Phone: +81 3 5769 5100

Taiwan
Dialog Semiconductor Taiwan
Phone: +886 281 786 222

Web site:
www.dialog-semiconductor.com

Hong Kong
Dialog Semiconductor Hong Kong
Phone: +852 2607 4271

Korea
Dialog Semiconductor Korea
Phone: +82 2 3469 8200

China (Shenzhen)
Dialog Semiconductor China
Phone: +86 755 2981 3669

China (Shanghai)
Dialog Semiconductor China
Phone: +86 21 5424 9058